FPGA_CONFIG

PLACE JTAG PROGRAMMING HEADER CLOSER THAN 10cm TO FPGA

PULL-UP IS REQUIRED BECAUSE PROG CABLES USES AN OPEN-DRAIN DRIVER TO CONTROL THE PGND SIGNAL FROM PLATFORM CABLE DOC PAGE

VCC1V8 — R19 1.5K 0.1% 0603

J1 — 0878311420 — MOLEX HEADER VERT 14POS 2MM

DGND 1, 3, 5, 7, 9, 11, 13 — 2, 4, 6, 8, 10, 12, 14

JTAG_TMS — R597 100
JTAG_TCK — R601 100
JTAG_TDO — R617 49.9
JTAG_TDI — R602 100 0603
NC
PS_SRST_B

JTAG PROGRAMMING HEADER (USING 1.8V)

HALT 14	13 PGND
NC 12	11 GND
TDI 10	9 GND
TDO 8	7 GND
TCK 6	5 GND
TMS 4	3 GND
VREF 2	1 GND

USB_JTAG_FLTR — USB_JTAG_VBUS

C833 1uF 25V 0603 — C258 0.1uF 50V 0402 — L62 — C257 0.1uF 50V 0402 — L63 — DGND

MPZ1608S300ATDH5

FERRITE BEAD, 30 OHM @ 100MHZ, 5A, 0603 1LN, -55C-125C

J19 USB 2.0 — USB_JTAG_VBUS 1, USB_JTAG_ID 4, USB_JTAG_DATA_P 3, USB_JTAG_DATA_N 2, USB_JTAG_GND 5 — S1 SHIELD1, S2 SHIELD2 — USB3090-30-A

MICRO USB 2.0 R/A RECP

TVS DIODE — TPD4S012DRYR — TVS DIODE 5.5V 6SON — USB_JTAG_VBUS

VCC1V8 — C1015 0.1uF 50V 0402

AUX3V3 — C1041 0.1uF 50V 0402

U69 — JTAG-SMT2-NC — 410-308-B — JTAG-SMT2-NC JTAG PROG MODULE, SMD

3V3, VREF, GND1, GND2, DM+, DP-, TMS, TCK, TDI, TDO, GPIO0, GPIO1, GPIO2_SRST — NC — SMT2_RSTST

PS_JTAG_TMS, PS_JTAG_TCK, PS_JTAG_TDI, PS_JTAG_TDO

VCC1V8 — R15 4.7K 0603

R687 0 0603

FROM RESET CIRCUIT — 8 PS_POR_B_1V8 — PS_POR_B_1V8

U17 — BUFFER OPEN DRAIN — SN74LVC07AMPWREP — LVOLT OPEN DRAIN NON-INV 6-CHAN BUFF TSSOP14 -55-125C

(1.65-5.5V) VCC, GND — 24mA 1=OPEN 0=CLOSED

C824 0.1uF 50V 0402

J2 — TSW-103-06-F-D — TSW-103-07-F-D

JTAG PROGMR JUMPER 3-4
USB PROGMR JUMPER 1-2
NORMAL JUMPER 5-6

VCC1V8 — R12 4.7K 0603

SEE TRACE_DEBUG BLOCK FOR PS_MODE BIT SETTINGS

VERSAL_POR_B_503

VCC1V8 — R22 1K 0603 — PUDC_B — B32 — PUDC_B_503_B32

U1 — VERSAL ACAP CONFIGURATION - BANK 503 — XCVM1802-2MSEVSVA2197 — ACAP VERSAL 1070MHZ 0.8V 2197-PIN BGA — 17 OF 25

(OPEN-DRAIN)

TMS_503_D30, TCK_503_D31, TDI_503_B31, TDO_503_C31

DONE_503_A33 — A33 — PS_DONE — 50 — PS_DONE
ERROR_OUT_503_A32 — A32 — PS_ERROR_OUT — 50 — PS_ERROR_OUT

TEMPERATURE-SENSING DIODE PINS
SYSMON_ROOT_DXN_500_AC32 — AC32 — FPGA_TEMP_DXN — FPGA_TEMP_DXN — 47
SYSMON_ROOT_DXP_500_AC33 — AC33 — FPGA_TEMP_DXP — FPGA_TEMP_DXP — 47

45mm x 45 mm x 3.71mm
1mm Pitch

RTC_PADI_503_B30 — B30
RTC_PADO_503_A30 — A30 — NC
RTC UNUSED NO CRYSTAL USED

POR_B_503_AE34 — AE34

(27- 60)Mhz (Optimum 33.3333MHZ))Mhz
REF_CLK_503_AE32 — AE32 — PS_REF_CLK — PS_REF_CLK — 20

(ASYNC RESET TO CONFIG LOGIC)

PS MIO MODE SELECT MODE PINS (MODE[3..0]) SAMPLED ON RISING EDGE OF PS_POR_B - see

MODE0_503_C32 — C32 — PS_MODE0 — 50 — PS_MODE0
MODE1_503_E32 — E32 — PS_MODE1 — 50 — PS_MODE1
MODE2_503_E31 — E31 — PS_MODE2 — 50 — PS_MODE2
MODE3_503_E30 — E30 — PS_MODE3 — 50 — PS_MODE3

(TIE TO GND OR VCCINT)
0=WEAK PRECONFIG I/O PULL-UP RES ENA
1=WEAK PRECONFIG I/O PULL-UP RES DISENA

VCC1V8 — R14 4.7K 0603

SWITCH OPEN 1.8V LED OFF
SWITCH CLOSED 0.16V LED OFF

VCC1V8 — R7 4.99K, R8 4.99K, R9 4.99K, R10 4.99K

PS_MODE0 — 50 — PS_MODE0
PS_MODE1 — 50 — PS_MODE1
PS_MODE2 — 50 — PS_MODE2
PS_MODE3 — 50 — PS_MODE3

S4 — SDA04H1SBD — DIP SWITCH SPST 4POS 25mA 24V — ON_1, ON_2, ON_3, ON_4 — OFF_1, OFF_2, OFF_3, OFF_4

R20 499, R21 499, R23 499, R24 499 — 1% 0630

U68 — BUFFER OPEN DRAIN — SN74LVC07AMPWREP — LVOLT OPEN DRAIN NON-INV 6-CHAN BUFF TSSOP14 -55-125C

AUX3V3 — R131 1K, R481 1K, R661 1K, R665 1K 0603

LED BLUE VF 2.65V, 2mA, 0603, -40C-85C
APT1608LVBC/D

PSMODE0 — D25 — MODE0
PSMODE1 — D26 — MODE1
PSMODE2 — D27 — MODE2
PSMODE3 — D28 — MODE3

VCC1V8 — C721 0.1uF 50V 0402

PLEASE ADD ON SILKSCREEN BOOT MODE POSSIBILITIES

SD CARD	PS QSPI BOOT-32- (SINGLE DEVICE)	PS BOOT JTAG
PS_MODE[3..0] = "0 1 0 1"	PS_MODE[3..0] = "0 0 1 0"	PS_MODE[3..0] = "0 0 0 0"
1 = UP	1 = UP	1 = UP
2 = DOWN	2 = UP	2 = UP
3 = UP	3 = DOWN	3 = UP
4 = DOWN	4 = UP	4 = UP

54,8 — RESET_1V1 — RESET_1V1
54 — HDMI_TXLOCKED — HDMI_TXLOCKED
PS_ERROR_OUT — 50 — PS_ERROR_OUT
PS_DONE — 50 — PS_DONE
8 — MCU_SANITY_CHECKER — MCU_SANITY_CHECKER — R48 10K — MCU_SANITY_1V8 13 — R49 6.04K

U39 — BUFFER OPEN DRAIN — SN74LVC07AMPWREP — LVOLT OPEN DRAIN NON-INV 6-CHAN BUFF TSSOP14 -55-125C

C43 0.1uF 50V

PSERROR_OUT
PSDONE
PSSANITY_CHECKER

AUX3V3 — R4 1K 0603, R3 1K 0603, R2 1K 0603, R1 1K 0603, R213 1K 0603

D8 RST1V8 — RED ON - RESETTING — LED RED VF 1.8V, 2mA, 0603, -40C-85C

D45 HDMI_TX_LCK

D2 PS_ERR — LED YELLOW VF 1.85V, 2mA, 0603, -40C-85C — YELLOW ON - POWER, HARDWARE, OR EXCEPTION ERROR

D3 PS_DONE — LED GREEN, VF 2.65V, 2mA, 0603, -40C-85C — GREEN ON - FPGA LOAD SUCCESFULLY COMPLETED

D4 PS_SANITY — GREEN ON/OFF - SANITY CHECKER 1s TOGGLE

DISTRIBUTION STATEMENT

FPGA CONFIGURATION

SIZE	FSCM NO.	DWG NO.	
D	12934		
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