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AXI PS/2 1.0 IP Core User Guide

Revised February 13, 2018; Author Sergiu Arpadi

1 Introduction

This user guide describes the Digilent AXI PS/2 Intellectual Property. The purpose of this IP is to implement a software controllable PS/2 host controller.

IP quick facts	
Supported device families	Zynq®-7000, 7 series
Supported user interfaces	Xilinx: AXI4 Lite, PS/2
Provided with core	
Design files	VHDL
Simulation model	N/A
Constraints file	XDC
Software driver	Standalone
Tested design flows	
Design entry	Vivado™ Design Suite 2016.4
Synthesis	Vivado Synthesis 2016.4

2 Features

- Contains two 16-byte deep FIFOs; one for TX and one for RX
- Generates a level sensitive interrupt depending on the IER register.
- Implements 7 AXI4 Lite registers for data, control, status and interrupt configuration.

3 Performance

The PS/2 IP Core is an AXI4 Lite PS/2 host controller capable of interfacing with either a mouse or a keyboard.

Sending data to a device is done by writing one byte at a time to the TX data register. The core then passes the bytes to the TX FIFO and determines when to send them to the PS/2 controller where they are serialized.

When a byte is received from the PS/2 device it is deserialized and stored in the RX FIFO from where it is passed to the RX data AXI4 Lite register.

An interrupt can be generated for certain situations like PS/2 communication errors or FIFO occupancy.

The core can also be reset from the software using the software reset register.

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4 Overview

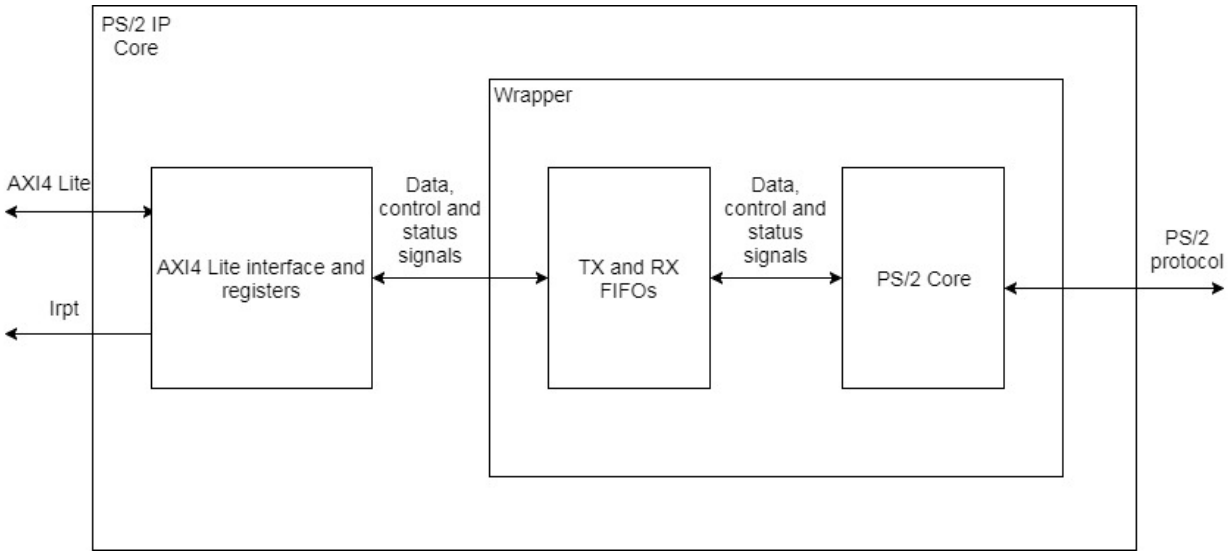

Figure 1. AXI PS/2 block diagram.

The IP consists of three main blocks. The AXI4 Lite block manages the control and status registers and is also in charge of generating the interrupt. The two FIFOs act as a buffer between this block and the PS/2 core where the PS/2 interface is implemented.

4.1 PS/2 protocol

The PS/2 protocol is a synchronous, serial, open drain, host to device protocol, the host consisting in this case of the FPGA via the AXI PS/2 IP and the device being either a mouse or keyboard.

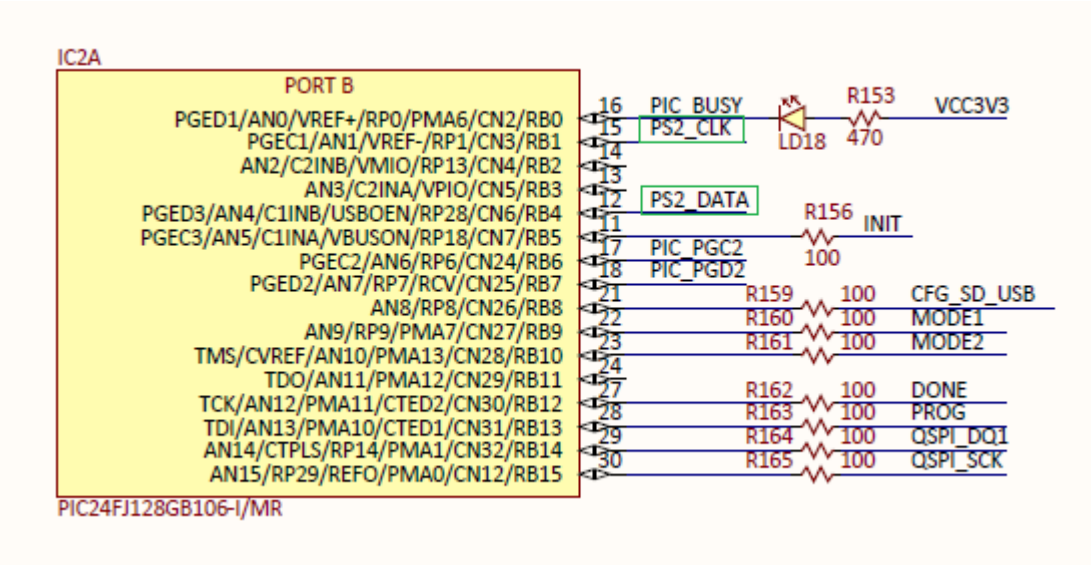

Figure 2. AXI PS/2 signals.

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Several Digilent boards including the Nexys4, Nexys4DDr, Genesys2, Nexys Video feature USB HOST connectors which are controlled by a PIC24 microcontroller which, among other functions, also converts the USB protocol to PS/2 and so, provides a connection to the FPGA. The IP core was designed to meet the PS/2 protocol specifications. Any device connected to the IP core must also comply to the PS/2 protocol.

Since there are no actual pull-up resistors on the two signals, PS2_DATA and PS2_CLK, internal pull-ups need to be activated in the FPGA for the interface to work.

4.2 AXI4 Lite registers

In total the AXI PS/2 core implements seven registers as listed below. The reason behind this configuration is the XPS PS2 IP core which is an IP provided by Xilinx for the older EDK platform. Although there are several differences between the two IPs, because of this similarity, it was possible to use most of the XPS PS2 driver.

Address Space Offset	Name	Description
00h	SRST	Software reset
04h	STS	Status register
08h	RX Data	Receive data register
0Ch	TX Data	Transmit data register
10h	GIE	Global interrupt enable
14h	ISR	Interrupt status register
18h	IER	Interrupt enable register

Table 1. AXI4 Lite register space

4.2.1 Software reset register

The SRST register is an internal write-only register which allows the software to reset the AXI PS/2 IP core. Writing 0xA to the register will reset all the logic including the two internal FIFOs. After the reset, the IP will return to its default state.

SRST

31	0

4.2.2 Status register

The status register provides information regarding the occupancy of the internal FIFOs using two bits for each FIFO. The TX/RX Empty bit is asserted when the TX/RX FIFO is empty, and the TX/RX Full bit is asserted when the TX/RX FIFO is full. Both FIFOs have a depth of 16 bytes. The register is read-only, and its reset value is 0xA.

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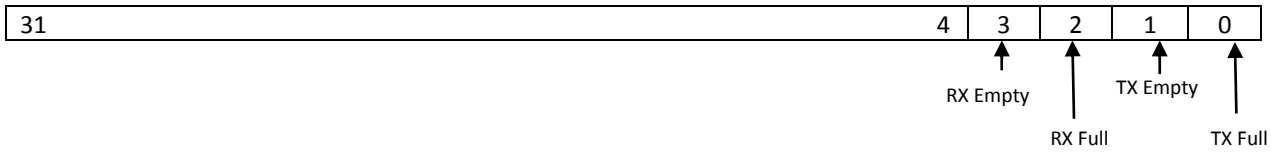
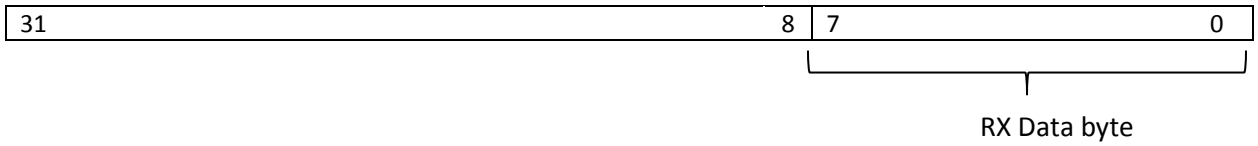
STS



4.2.3 RX Data register

The RX Data register stores data that was received from the PS/2 device after being validated by the PS/2 logic. The register will not contain data which was invalidated. When data is read from the register, new data will be automatically loaded from the RX FIFO if data is available. When the RX FIFO is empty and new data is received, it will be written into the RX Data register; the FIFO is first-word-fall-through. The register is read-only, reset value is 0.

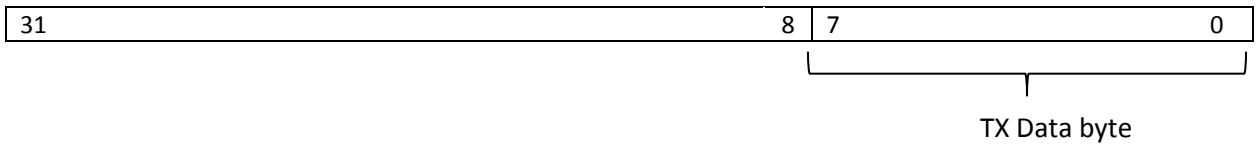
RX Data



4.2.4 TX Data register RW

This register is used for sending data to the PS/2 interface. Simply by writing a byte to the register, it will be passed to the TX FIFO, if the FIFO is not full at that point. It is recommended that the status register should be read before sending a new byte, to avoid data loss. The TX FIFO ensures that the PS/2 logic has time to process bytes that are being sent and acts as a buffer since the protocol is very slow in comparison. When the PS/2 logic becomes idle, the next available data byte is extracted from the FIFO. This is a write-only register, reset value is 0.

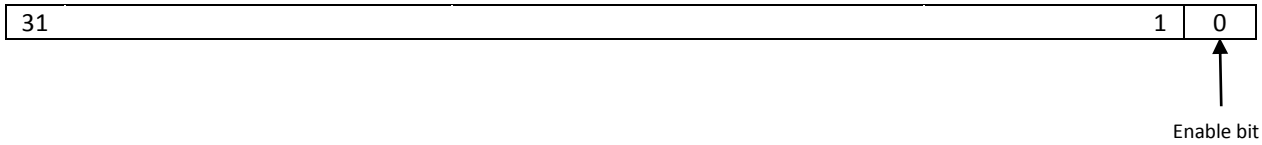
TX Data



4.2.5 Global interrupt register RW

The GIE register enables the interrupt signal generated by the when bit 0 is set to ‘1’. When bit 0 is ‘0’, the interrupt is disabled. Write-only register, reset value is 0.

GIE



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4.2.6 Interrupt status register RW

The ISR indicates the reason why the interrupt was generated. The register provides write-to-clear access and so, it avoids the requirement on the user interrupt service routine to perform Read-Modify-Write operation to clear the status bit of the interrupt. Read-Modify-Write operations can lead to inadvertent clearing of interrupts captured in the time between the read and write operations. Therefore, to clear an interrupt, 1 must be written to the corresponding bit in the ISR, while writing 0 to the others.

There are 5 situations when an interrupt is generated.

Tx Noack – Acknowledge not received from the PS/2 device after byte transmission. Indicates communication error.

Tx Ack – Acknowledge was received from the PS/2 device after byte transmission. Indicates successful transmission of data.

Rx Ovf – Indicates that data was received from the PS/2 device while the RX FIFO was full. In this situation, the logic attempts to write data to the FIFO when it can no longer accept data. This indicates data loss.

Rx Err – Received data with parity error. In this case the byte will not be written into the RX Data register. This indicates that a byte failed to be received by the IP.

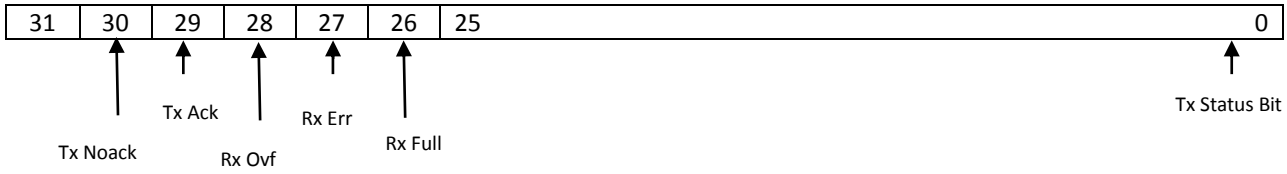
Rx Full – Indicates that data is available to be read from the RX Data register. It does not imply that the FIFO is full. This interrupt can only be cleared by reading the data available.

The ISR has a reset value of ‘0’ and is a read-write register.

4.2.7 Interrupt enable register RW

The IER allows the software to enable the interrupts independently of eachother by writing ‘1’ to the corresponding bit. It has the same structure as the ISR, reset value is 0

ISR/IER



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4.3 Transfer control

As stated above, there are 3 main blocks which make up the AXI PS/2 IP core. The PS/2 protocol is implemented in one of these blocks and is controlled by using the AXI Lite registers. The main logic consists of a state machine which branches in two directions, TX and RX. Besides the actual data processing, several other signals are used which indicate either a transmission error, parity error or the existence of the acknowledge bit.

The interrupt signal is generated in the first block which is also in charge of implementing the registers. It is basically a logical OR between the ISR bits which have been enabled by the IER register. To clear an interrupt, a 0 must be written in the ISR at the corresponding bit. All the interrupts are software resettable except for the “RX_FULL” interrupt which can only be cleared by reading data from the core. The interrupt will always be generated when data is available in the RX_DATA register and the interrupt is enabled.

5 Port descriptions

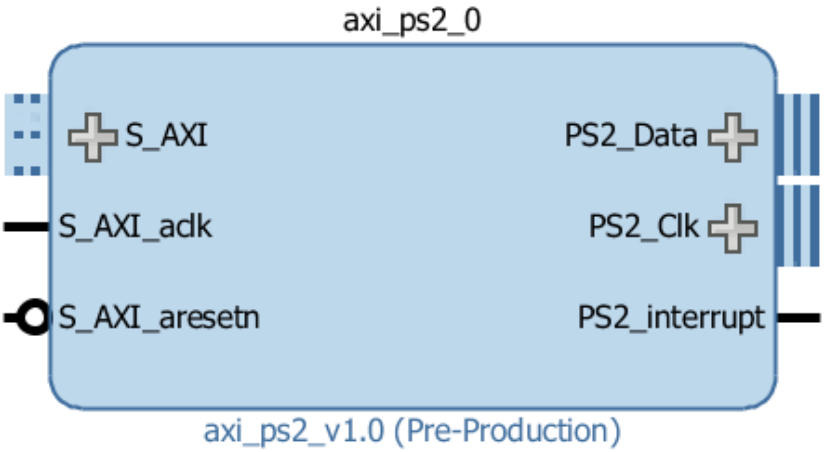

Figure 2. AXI PS/2 IP Core.

The table below will present the signals and interfaces implemented by the PS/2 core.

Signal Name	Signal Type	Description
S_AXI _aclk	Input	AXI4 Lite interface clock signal
S_AXI _aresetn	Input	AXI4 Lite reset signal
PS2_interrupt	Output	Interrupt signal driven by the core

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AXI4 Lite Interface signals		
S_AXI	Input / Output	AXI4 Lite interface used to communicate with the core's registers
PS/2 Protocol signals		
PS2_Data	Inout	PS/2 data signal
PS2_Clk	Inout	PS/2 clock signal

Table 2. Port descriptions

6 Designing with the core

6.1 Constraints

Since there are no actual pull-up resistors on the two signals, PS2_DATA and PS2_CLK, internal pull-ups need to be activated in the FPGA for the interface to work.

7 References

The following documents provide additional information on the subjects discussed:

1. Xilinx Inc., *DS707: LogiCORE IP XPS PS2 Controller (v1.01b), April 19, 2010*
2. http://www.computer-engineering.org/ps2protocol/
3. http://www.computer-engineering.org/ps2keyboard/

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